An 8-b 1-GS/s CMOS Cascaded Folding and Interpolating ADC

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Abstract — This paper presents an 8-bit low power cascaded folding and interpolating analog-to-digital converter (ADC). A reduction in the number of comparators, equal to the number of times the signal is folded, is obtained. The interleaved architecture is used to improve the sampling rate of the ADC. The circuit including a bandgap is implemented in a 0.18-μm CMOS technology, and measures 1.47 mm × 1.47 mm (including pads). The simulation results illustrate a conversion rate of 1-GS/s and a power dissipation of less than 290 mW.

Index Terms — Analog-to-Digital converter, CMOS analog integrated circuit, folding-and-interpolating, cascading.

I. INTRODUCTION

Analog to digital converters (ADCs) play an important role in a variety of applications. They are used to convert an analog value into a digital word that can be transmitted or processed by a digital processing system. To take advantage of the increasing speed and sophistication of digital signal processing, the ADCs must operate at high sampling rates and low voltage. The flash architecture shows a good speed performance and can easily be implemented in an integrated circuit as a repetition of simple comparator blocks and a ROM decoder structure [1]. However, this architecture requires \(2^N\)-1 comparators to achieve N-bit resolution, which results in a substantial area and power penalty starting at the 8-b level.

This paper describes the design of an 8-bit 1 GS/s with an on-chip track-and-hold amplifier (THA) using the 0.18-μm CMOS. To achieve the low power consumption and low power supply voltage, a cascaded folding-interpolating architecture is proposed.

II. ADC ARCHITECTURE

The block diagram of the ADC is illustrated in Fig. 1. The THA, folding amplifiers 1 and 2, comparators, coarse comparators, and encoder are all interleaved by two, running at 500 MHz for this nominally 1-GS/s differential ADC.

A. Interleaved THA

The THA at the front-end of the converter performs the time sampling of the input signal. An open-loop topology was chosen because of the very high conversion speed. A simplified circuit diagram of one slice of the interleaved THA circuit is given in Fig. 2. It consists of input buffers, sampling switches, and output buffers. The differential input buffer consists of a differential pair M1 and M2 with tail current sources I1 and I2. The differential input signals are applied to the gates of the resistors M1 and M2. The differential output of the input buffer goes to the track-and-hold switches. Each track-and-hold switch consists of the main switch M3, a dummy switch M9, a holding capacitor (CH) and a bootstrap capacitor (CB). In the track phase, the boost capacitor CH previously charged to VON is connected between gate and source of the sampling transistor M3, thus acting as a battery and providing an almost constant gate-to-source voltage [2], which makes the sampling signal-independent. The dummy switch M9, with the source and drain connected together, is driven by clock H such that after M3 turns off and M9 turns on, the channel charge deposited by the former on CH is absorbed by the latter to create a channel. Choosing the proper size of M3 and M9, the effect of clock feedthrough and charge injection is weakened. The output buffer consists of a differential pair of PMOS source follows M17 and M18 with their bodies connected to their sources [3].
B. Folding-and-Interpolating Amplifier

The cascading scheme achieves a high folding degree while avoiding the high gain and/or bandwidth requirements of each folder [4]. The output of the track-and-hold circuit is applied to the input of the 1st step folding amplifiers with a folding factor of 3 which is combined by the nine folding blocks, and coarse comparators. A reference ladder is used to generate a set of reference voltages. Fig. 3(a) shows the topology of the 1st folding amplifier used in this implementation. The amplifier whose reference voltage is close to the input voltage is "active", while the two amplifiers not close to a crossing point are saturated and do not influence the comparator decision. The basic function performed by the folding amplifiers is the conversion of the increasing (or decreasing) input signal into a number of sinusoid-like output signals [5]. Each folding amplifier generates three zero-crossing, equidistantly spaced over the input range. Nine folding amplifiers are used in parallel, generating 27 zero-crossing. To ensure that the ADC achieves the required resolution, accurate zero-crossing points must be generated by the folding circuits. In order to reduce the mismatch between M1 and M2 in each differential pair, these transistors should be large enough, but increasing the size of these transistors affects the loading capacitance of the previous stage, so there should be a compromise in choosing the size of M1 and M2. In this design, the size of these transistors was chosen to be $0.35 \times 5 \ \mu m^2$ [6]. The output of the 1st step folding amplifiers is a set of phase-shifted sinusoid-like signals which are, in turn, applied to the input of the 2nd step folding amplifiers. The topology of the 2nd step folding amplifiers used in this implementation is shown in Fig. 3(b). The 2nd step folding amplifiers fold the output signals of the 1st step folding amplifiers by the factor of three. In each of these arrays, $9 \times 3$ differential pairs are joined at the load into nine amplifier triplets, each sharing a common load, whose outputs are interpolated and made
available to the following stage. The interpolation is implemented using a resistive string because of its simplicity and power efficiency. In this design, differential interpolation is implemented by applying the differential outputs of the folding amplifiers to the differential resistive strings. This differential implementation improves the accuracy of the converter.

C. Comparator
The topology of the comparator used in this implementation is shown in Fig. 4. During the comparing phase, the voltage difference between the input signals Vin+ and Vin− causes the different current follow through the differential pair of transistors M5 and M6 which, in turn, make the voltage of VA and VB change in the opposite direction. The transistors M7, M8, M9, and M10, connected in a positive-feedback configuration, latch the differential signal. Such a comparator architecture reduces the kickback noise to an acceptably low level. Another advantage of this architecture is that it nearly consuming no power during the phase of reset. Besides, it is very suitable for the low power voltage system because there are only three transistors paralleled between the supply voltage and ground.

D. Encoder and Error Correction
The digital encoder is comprised of two functional blocks: a logic array and a 256-to-8 ROM which is divided into four parts for the reason of driving capability. To deduce the influence of the bubble, three input NAND gates and the method of Gray encode are used as illustrated in Fig. 5.

III. SIMULATION RESULTS AND LAYOUT
In high frequencies, the accuracy of the converter decreases mainly due to the timing mismatches between different parts designed in 0.18-µm 1P6M Mixed-signal CMOS technology of the circuit. To minimize timing mismatches, a tree-structure was used for layout of the clock and analog signal paths to make sure the wiring for each of the clock and signal paths in the layout is symmetrical. The proposed ADC with single 1.8V supply has been simulated with spectrm. The layout of the ADC is shown in Fig. 6. The chip area including pads is 1.47mm × 1.47mm. Simulation indicates its power consumption is less than 290 mW. A part of the differential
A 8-bit, 1-MSample/s, Folding-and-Interpolating ADC is designed. To reduce the number of comparators, power consumption and increase input bandwidth, a new cascading architecture is proposed. The total number of comparators is (1.47mm×1.47mm in 0.18μm CMOS) ADC. Design results are summarized in Table 1.

### Table 1. Simulation results of proposed ADC

<table>
<thead>
<tr>
<th>Resolution</th>
<th>8 bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conversion Speed</td>
<td>1-MS/s</td>
</tr>
<tr>
<td>Power supply</td>
<td>1.8V</td>
</tr>
<tr>
<td>Power consumption</td>
<td>&lt;290mW</td>
</tr>
<tr>
<td>DNL/DNL</td>
<td>0.8LSB/0.6LSB</td>
</tr>
<tr>
<td>Technology</td>
<td>0.18μm 1P6M CMOS</td>
</tr>
<tr>
<td>Chip area</td>
<td>1.47mm×1.47mm</td>
</tr>
</tbody>
</table>

output of the Cascading Folding-and-Interpolating circuit is shown in Fig. 7. The simulation result from the encoder is illustrated in Fig. 8. The differential nonlinearity (DNL) and integral nonlinearity (INL) of the converter are illustrated in Fig. 9. From the graph, the converter exhibits a maximum value of 0.6 and 0.8 LSB for DNL and INL, respectively.

### IV. CONCLUSION

A 8-bit, 1-MSample/s, Folding-and-Interpolating ADC is designed. To reduce the number of comparators, power consumption and increase input bandwidth, a new cascading architecture is proposed. The total number of comparators is (1.47mm×1.47mm in 0.18μm CMOS) ADC. Design results are summarized in Table 1.

### REFERENCES


