Structure optimization of field-plate AlGaN/GaN HEMTs

Weijun Luoa,b,*, Ke Weib, Xiaojuan Chenb, Chengzhan Lib, Xinyu Liub, Xiaoliang Wanga

a Institute of Semiconductor of Chinese Academy of Sciences, Beijing 100083, China
b Institute of Microelectronics of Chinese Academy of Sciences, Beijing 100029, China

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Abstract

AlGaN/GaN high electron mobility transistors (HEMTs) on 6H-SiC with varying field-plate length and gate–drain spacing were fabricated and analyzed. The classical small signal FET model and the well-known ColdFET method were used to extract the small signal parameters of the devices. Though the devices with field plates exhibited lower better \(f_T\) characteristic, they did demonstrate better \(f_{\text{max}}\) MSG and power density performances than the conventional devices without field plate. Besides, no independence of DC characteristic on field-plate length was observed. With the increase of the field-plate length and the gate–drain spacing, the characteristic of \(f_T\) and \(f_{\text{max}}\) degraded due to the large parasitic effects. Loadpull method was used to measure the microwave power performance of the devices. Under the condition of continuous wave at 5.4 GHz, an output power density of 4.69 W/mm was obtained for device with field-plate length of 0.5 \(\mu\)m and gate–drain length of 2 \(\mu\)m.

Keywords: GaN; HEMT; Field plate; Small signal; Power

1. Introduction

GaN-based high electron mobility transistors (HEMTs) have great potential for next generation high-power, high-temperature devices and wireless base station amplifiers application. Recently, AlGaN/GaN HEMTs on silicon carbide (SiC) substrates have demonstrated a power density of 32 and 16.5 W/mm under the condition of 4 and 10 GHz, respectively. [1,2] In order to investigate its potential of high power, it is of great importance to improve the breakdown voltage of the AlGaN/GaN HEMTs. Under the operation of high bias voltage, however, many microwave experiments of these devices are not good as expected from their DC performance. This may be mainly due to the RF dispersion under the large-signal microwave condition, as well as the reverse Schottcky-gate leakage current.

In recent years, field plates were used to enhance the microwave performances of the GaN-based HEMTs. With field plates, the breakdown voltage, stability, reliability, surface trap effects, and linearity of the device were improved a lot, then a large output power density can be obtained. [3–5] In this paper, three kinds of field-plate devices with different geometry structure parameters are fabricated and tested. Comparisons of the devices with different field plates as well as the conventional structure without field plates are carried out. The results show that with proper field–plates, the AlGaN/GaN HEMTs demonstrated a more stable, high breakdown voltage and high power density performance.

2. Epitaxial layer structure and device processing

The epitaxial layer used in this paper was grown by metal organic chemical vapor deposition (MOCVD) on 6H-SiC substrate. The layer consists of a AlN buffer layer, an undoped 3 \(\mu\)m GaN layer, and a 20 nm AlGaN barrier layer. The devices were fabricated using standard optical lithography techniques. Three types of source terminated field-plate devices are developed and named with A, B, and C, respectively. Silicon nitride was deposited under the field plates using plasma-enhanced chemical
vapor deposition (PECVD), whose thickness is 300 nm. The conventional structure, without field plates is also fabricated named with N. With the same gate length, $L_g = 0.8 \mu m$, and gate width, $W_g = 120 \mu m$, the parameter differences of the four kinds of devices can be seen from Table 1.

3. Results and discussion

According to the on-wafer DC data, there is no obvious difference among the four kinds of devices. The small signal RF performance, however, is not the same. By using the HP8510C network analyzer and agilent ICCAP system, the small signal RF performances of the devices under different bias condition were tested and analyzed. To examine the RF performance of the devices, the small signal parameters of the devices were extracted by using the classical small signal FET model and the well-known ColdFET method. [6–8] The small signal equivalent circuit of the FET is depicted in Fig. 1. The main parasitic parameters as well as intrinsic parameters of the devices are showed in Table 2.

Based on the classical small signal FET model, the gate–drain spacing, $L_{GD}$ mainly influence the $R_d$, $L_d$, and $C_{gd}$. [9] Seen from the Table 2, $R_d$ and $L_d$ increased with the $L_{GD}$, while $C_{gd}$ decreased. The unity-gain cut-off frequency ($f_T$), the maximum frequency of oscillation ($f_{max}$) and the maximum stable gain (MSG) characteristics of the devices under different source–drain voltages are depicted in Figs. 2 and 3. Under the gate voltage of $-3 \text{ V}$, all the devices with source terminated field plate exhibit lower $f_T$, no matter how much the source–drain voltage is. This is mainly due to the large parasitic parameters of the field-plate structures, which are illustrated in Table 2. However, $f_{max}$ of the conventional structure is not the best one. As illustrated in Figs. 2 and 3, the source terminated field-plate structures demonstrated a higher and increasing $f_{max}$ and MSG. Because, the electric enhancement in the two-dimensional electron gas (2DEG) channel between the gate and drain electrode can be reduced a lot by using the field plates. Thus, a more stable gain under the high bias voltage can be obtained. As to the three field-plate structures, the structure C shows the lowest $f_T$, which

<table>
<thead>
<tr>
<th>$L_{GD}$ ($\mu m$)</th>
<th>$L_{FP}$ ($\mu m$)</th>
<th>$L_{SD}$ ($\mu m$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>2.2</td>
<td>0.5</td>
</tr>
<tr>
<td>B</td>
<td>2.0</td>
<td>0.5</td>
</tr>
<tr>
<td>C</td>
<td>2.6</td>
<td>0.7</td>
</tr>
<tr>
<td>N</td>
<td>1.6</td>
<td>0</td>
</tr>
</tbody>
</table>

Table 2
Parasitic parameters of the devices

<table>
<thead>
<tr>
<th></th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>N</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_d \Omega$</td>
<td>6.1</td>
<td>5.6</td>
<td>7.2</td>
<td>8.2</td>
</tr>
<tr>
<td>$R_g \Omega$</td>
<td>7.6</td>
<td>7.5</td>
<td>7.6</td>
<td>5.4</td>
</tr>
<tr>
<td>$R_s \Omega$</td>
<td>0.3</td>
<td>0.8</td>
<td>0.98</td>
<td>6.1</td>
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<tr>
<td>$L_d \text{nH}$</td>
<td>99.9</td>
<td>94.4</td>
<td>100.6</td>
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</tr>
<tr>
<td>$L_g \text{nH}$</td>
<td>109.5</td>
<td>115.3</td>
<td>112.1</td>
<td>83.1</td>
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<tr>
<td>$L_s \text{nH}$</td>
<td>98.1</td>
<td>100.1</td>
<td>97.0</td>
<td>114.8</td>
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<tr>
<td>$C_{gd} \text{fF}$</td>
<td>36.4</td>
<td>36.3</td>
<td>41.9</td>
<td>34.5</td>
</tr>
<tr>
<td>$C_{pg} \text{fF}$</td>
<td>48.0</td>
<td>46.8</td>
<td>51.3</td>
<td>9.8</td>
</tr>
</tbody>
</table>

Fig. 1. The classical small signal FET model.

![Fig. 1. The classical small signal FET model.](image)

Fig. 2. The unity-gain cut-off frequency ($f_T$) and the maximum frequency of oscillation ($f_{max}$) characteristics of the devices under different source–drain voltages.

![Fig. 2. The unity-gain cut-off frequency ($f_T$) and the maximum frequency of oscillation ($f_{max}$) characteristics of the devices under different source–drain voltages.](image)

Fig. 3. Maximum stable gain (MSG) characteristics of the devices under different source–drain voltages.

![Fig. 3. Maximum stable gain (MSG) characteristics of the devices under different source–drain voltages.](image)
may caused by the trapping effects deteriorated with the increasing of $L_{GD}$. And the lowest MSG of the structure C mainly due to the large drain electrode resistance, $R_d$, which also increased with the $L_{GD}$ [9]. Then the RF loss is to be increased, too.

With the longest field plate, $L_{FP}$, the structure C shows a lowest $f_T$, $f_{max}$, and MSG. It is mainly caused by the large parasitic effects exacerbating with the $L_{FP}$, which can be deduced from the small signal parasitic parameters as described in Table 2. On the other hand, both the $f_{max}$ and MSG of the structure C exhibited an up-trend with the increasing of source–drain voltage. It means that the structure C has potential to be operated at large voltage, because of the gently electric enhancement in the channel due to the large $L_{FP}$ and $L_{GD}$.

Large-signal microwave power measurements were performed using a focus microwave load-pull system. Under the continuous wave (CW) of 5.4 GHz, the devices were biased at different drain voltages to test their output power. After the automatic tuning by the tuner, the maximum output power and the power gain of the devices were described in the Fig. 4. At the drain bias of 40 V, power densities of 3.24, 3.99, 4.37, and 4.69 W/mm were measured for devices N, C, A, and B, respectively. And the corresponding gains are 12.8, 14.3, 14.7, and 15.3 dB. All three source terminated field-plate structures demonstrated rapid increasing output power with the adding of the source–drain voltage. While the output power of the structure N saturates easily with the increase of the source–drain voltage. The same trend can be obtained from the power gain of the four devices. The power gain of the devices with field plates is larger and more stable than that of the device N. The reasons may be that the breakdown voltage, the surface trapping effect and the gate leakage current can be improved by using the field plates. So a more stable performance and high output power under the high source–drain voltage can be obtained. Among the three devices with field plates, the structure B exhibited the best performance, which agrees well with the small signal performance. It is believed that the parasitic effects are more obvious with the increasing of the field-plate length, which can be deduced from the parasitic parameters illustrated in Table 2. Thus, the loss and stability of the device will deteriorate. Besides, the gate–drain spacing, $L_{GD}$, is also an important structure factor. Because, the drain electrode parasitic resistance, $R_d$, as well as the trapping effects between the gate and drain electrode increase with the gate–drain spacing, $L_{GD}$.

4. Summary

In summary, we have presented the results of the AlGaN/GaN HEMTs with varying field-plate length and gate–drain spacing. The classical small signal FET model and the well-known ColdFET method were used to extract the small signal parameters of the devices. With the increase of the field-plate length and the gate–drain spacing, the characteristic of $f_T$ and $f_{max}$ degraded due to the large parasitic effects. Though, the devices with field plates exhibited lower better $f_T$ characteristic, they did demonstrate better $f_{max}$, MSG and power density performances than the conventional devices without field plate. Besides, no independence of DC characteristic on field-plate length was observed. At the frequency of 5.4 GHz, a CW output power density of 4.69 W/mm was obtained for device with field-plate length of 0.5 mm and gate–drain length of 2 μm.

Acknowledgments

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References