A Compact Direct Digital Frequency Synthesizer for System-on-chip

Cao Xiaodong¹, Ni Weining², Yuan Ling³, Hao Zhikun¹, Shi Yin¹
Institute of Semiconductors, Chinese Academy of Sciences, Beijing 100083, P. R. China
*Email: xdcao@semi.ac.cn

Abstract

A compact direct digital frequency synthesizer (DDFS) for system-on-chip (SoC) is developed in this paper. For smaller chip size and lower power consumption, the phase to sine mapping data is compressed by using sine symmetry technique, sine-phase difference technique, quad line approximation (QLA) technique and quantization and error read only memory (QE-ROM) technique. The ROM size is reduced by 98% using the techniques mentioned above. A compact DDFS chip with 32-bit phase storage depth and a 10-bit on-chip digital to analog converter (DAC) has been successfully implemented using standard 0.35um CMOS process. The core area of the DDFS is 1.6mm². It consumes 167 mW at 3.3V, and its spurious free dynamic range (SFDR) is 61dB.

1. Introduction

Direct digital frequency synthesizers (DDFSs) are important to modern communication systems. DDFSs are able to generate single-phase or quadrature sinusoids with excellent frequency resolution, good spectral purity, very fast frequency switching and phase continuity on switching [1]. Generally, a DDFS consists of a phase accumulator, a phase to sine converter (sine ROM), and a DAC. For higher access speed, higher reliability, smaller chip size and lower power consumption, several ROM size reduction algorithms are used in this paper. The most elementary technique of compression is to store only \( \frac{\pi}{12} \) rad of sine information, and to generate the ROM samples for the full range of \( 2\pi \) by exploiting the quarter-wave symmetry of the sine function [2]. The quarter wave memory can be further compressed by using modified Sunderland technique, sine-phase difference technique, Quad line approximation (QLA) technique, and quantization and error ROM (QE-ROM) technique. The phase of a quarter of a sine wave can be decomposed as \( \Phi = \alpha + \beta + \gamma \), where \( \alpha \), \( \beta \), and \( \gamma \) are, respectively, the most significant bits (MSBs), the middle bits, and the least significant bits (LSBs). The whole compression process in this paper is depicted in Fig.1.

A 10-bit on-chip current steering DAC is also implemented to convert the digital amplitude word to equivalent analog amplitude.

2. Phase accumulator

The phase accumulator is based on a 32-bit ripple carry adder, with a string of full adders that all operate on the same clock phase. The outputs of the full adders have built-in registers, and the sum bits feed back internally to perform accumulation. A multiplexer (MUX) is used to select the phase increment word from the 32-bit phase increment words stored in registers. In order to guarantee the phase continuity, the select signal should be synthesized with the system clock signal of the DDFS.

3. Phase to sine converter

3.1 Sine function symmetry technique

The full-period sine wave can be reconstructed with only \( \pi/2 \) rad of sine information by exploiting the quarter-wave symmetry of the sine function. Fig.2 shows the details of this method. Since the most significant two bits of the phase accumulator represent the quadrant of the sine function, the most significant bit (MSB) is used as the sign bit of the result, and the second most
important bit (2nd MSB) is used to control whether the phase should be increasing or decreasing \cite{3}. The low j-2 bits of the phase accumulator output are sent to a complementor controlled by the 2nd MSB to generate addresses for the quarter-sine ROM. The slope of the saw tooth is inverted for the second quadrant. The waveform at the output of the quarter-sine ROM is the quantified sine wave. The full-period sine wave is generated at the output of the second complementor, which consists of m-1 exclusive-or gates and an inverter.

3.2 Modified Sunderland technique

To reduce the ROM size, this DDFS utilizes the modified Sunderland technique based on simple trigonometric identities \cite{4}. The phase address of a quarter of a sine wave can be decomposed as \( \Phi = \alpha + \beta + \gamma \), where \( \alpha \) is the MSBs, \( \beta \) is the middle bits, and \( \gamma \) is the LSBs. The quarter-wave sine function is given by

\[
\sin\left(\frac{(\alpha+\beta+\gamma)\pi}{2^j}\right) = \sin\left(\frac{(\alpha+\beta)\pi}{2^j}\right) \cos\left(\frac{\gamma\pi}{2^j}\right) + \cos\left(\frac{(\alpha+\beta)\pi}{2^j}\right) \sin\left(\frac{\gamma\pi}{2^j}\right)
\]

Where \( j \) is the number of the phase accumulator output bits. Equation (1) can be simplified further to

\[
\sin\left(\frac{(\alpha+\beta+\gamma)\pi}{2^j}\right) = \sin\left(\frac{(\alpha+\beta)\pi}{2^j}\right) + \cos\left(\frac{(\alpha+\beta)\pi}{2^j}\right) \sin\left(\frac{\gamma\pi}{2^j}\right)
\]

The information of the first term on the right of Equation (2) is stored into a coarse ROM. The second term on the right of Equation (2) is stored into a fine ROM. This method works by introducing the 1/2LSB offsets into the phase and amplitude of the sine ROM samples. However, significant savings in ROM size can be realized due to the small magnitudes of \( \beta \) and \( \gamma \) relative to \( \alpha \). The 10-bit phase data of accumulator outputs is divided into three parts in this design. Computer simulations determine the optimum partitioning ratio \( \alpha = 4, \beta = 3 \) and \( \gamma = 3 \).
3.5 QE-ROM technique

Based on the continuity of the data that need compressing, the ROM size of the DDFS can be further reduced by using the QE-ROM technique. In this design, the second term on the right of Equation (2) and \( cr(a+\beta) \) are both compressed by using the QE-ROM technique. The ROM size can be reduced to \( 2^l \times m + 2^a \times n \) bits using QE-ROM technique, where \( l, m, a, \) and \( n \) are, respectively, the length of the address of the quantization ROM, the length of the data in the quantization ROM, the length of the address of the original data and the length of the data in the error ROM. It can be known from calculations that the minimum size of the coarse ROM for a 10-bit output DDFS is 480 bits \( (2^5 \times 3 + 2^7 \times 3 = 480) \). The second term on the right of Equation (2) is stored into a fine ROM which is also divided into a quantization ROM and an error ROM by using QE-ROM technique. The minimum size of the fine ROM for a 10-bit output DDFS is 288 bits \( (2^5 \times 1 + 2^7 \times 2 = 288) \). So the total ROM size for a 10-bit sine output is only 768 bits.

3.6 Architecture of the phase to sine converter

Fig. 3 shows the block diagram of the phase to sine converter, which consists of complementsors, multiplexers (MUXs), ROMs, and adders. The complementsors are used for recovering the full wave output from the quarter sine ROM by inverting the phase and amplitude appropriately. Four column MUXs and three adders are also required. Fig. 4 shows the relative bit positions of the data used for reconstructing a sine wave. The first row represents the 7-bit phase, the second row represents the 7-bit quad line approximation, the third row represents the 3-bit quantization-ROM data in the coarse ROM, the fourth row represents the 3-bit error-ROM data in the coarse ROM, the fifth row represents the 1-bit quantization-ROM data in the fine ROM, the sixth row represents the 2-bit error-ROM data in the fine ROM, and the seventh row represents the 9-bit output of the adders in Fig. 4.

The DDFS requires smallest ROM size compared with the DDFS using other compression methods in Table 1. Moreover, this technique produces good spur level with less additional logic.

![Fig.3 Architecture of the phase to sine converter](image)

![Fig.4 Relative bit positions of data to be added in the adders](image)

Table 1. Summary of memory compression and algorithmic techniques in the case of 12-bit phase to 10-bit amplitude mapping

<table>
<thead>
<tr>
<th>Compression method</th>
<th>Needed ROM</th>
<th>Total compression ratio</th>
<th>Worst case spur (dBc)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Uncompressed Memory</td>
<td>( 2^{12} \times 10 )</td>
<td>1:1</td>
<td>-81.76</td>
</tr>
<tr>
<td>Quarter Sine Wave</td>
<td>( 2^{10} \times 9 )</td>
<td>40:9</td>
<td>-78.76</td>
</tr>
<tr>
<td>Double Trigonometric</td>
<td>( 2^{10} \times 6 )</td>
<td>20:3</td>
<td>-78.76</td>
</tr>
<tr>
<td>Modified Sunderland</td>
<td>( 2^7 \times 10 )</td>
<td>32:1</td>
<td>-73.59</td>
</tr>
<tr>
<td>Architecture</td>
<td>( 2^7 \times 9 )</td>
<td>320:9</td>
<td>-74.56</td>
</tr>
<tr>
<td>Modified Nicholas</td>
<td>( 2^7 \times 6 )</td>
<td>160:3</td>
<td>-66.8</td>
</tr>
<tr>
<td>Architecture</td>
<td>( 2^7 \times 6 )</td>
<td>160:3</td>
<td>-72.32</td>
</tr>
</tbody>
</table>
4. Digital to analog converter

In this design, an on-chip 10-bit segmented current steering digital to analog converter (DAC) is implemented. This converter has 6-bit thermometer-decoded most significant bits (MSBs) and 4-bit thermometer-decoded least significant bits (LSBs). It is full thermometer-decoded to guarantee monotonicity and minimal glitches. The simplified DAC architecture is shown in Fig.5. A clock buffer is included on the chip to obtain a good timing accuracy for the different clock signals used in the converter. A step-down buffer shown in Fig.6 has also been added in front of every current switch to achieve a better dynamic performance. Two important parameters of DACs' static performance are integral nonlinearity (INL) and differential nonlinearity (DNL), which are related to the strategy of the layout implementation. The DAC used in this paper employs a novel switching scheme called Q2 random walk to improve the nonlinearity, which can be degraded by the symmetric error and two-dimensional graded error of the DAC [7].

5. Layout and experiment result

The compact DDFS has been fabricated using 0.35um CMOS process. Fig.7 shows the chip micrograph. Besides the DDFS, some other circuits are also implemented on the same chip. Fig.8 shows a SFDR of 61dB at a system clock frequency of 20MHz.

6. Acknowledgments

A compact DDFS for SoC is implemented in this paper. The DDFS consists of two 32-bit phase registers, a 32-bit phase accumulator, a phase to sine converter (768-bit sin ROM) and a 10-bit on-chip DAC. A DDFS chip with a core area of 1.6mm² has been successfully fabricated using standard 0.35um CMOS process. The DDFS consumes 167 mW at 3.3V and its SFDR is 61dB.

References