A widely tunable continuous-time LPF for a direct conversion DBS Tuner

Bei Chen1, Fangxiong Chen1, Heping Ma1, Yin Shi1, Fa Foster Dai2
1 Institute of Semiconductors, Chinese Academy of Sciences, P.O.Box 912, Beijing, China
2 Elec. & Computer Eng. Department, Auburn University, Auburn, AL 36849-5201, USA
*Email: bchen@semi.ac.cn

Abstract

A continuous-time 7th-order Butterworth Gm-C low pass filter (LPF) with on-chip automatic tuning circuit has been implemented for a direct conversion DBS tuner in a 0.35um SiGe BiCMOS technology. The filter's -3dB cutoff frequency \( f_c \) can be tuned from 4MHz to 40MHz. A novel translinear transconductor (Gm) cell is used to implement the widely tunable and high linear filter. The filter has -0.5dB passband gain, 28mV/Hz\(^{1/2}\) input referred noise, -2dBVrms passband IIP3, 24dBVrms stopband IIP3. The I/Q LPFs with the tuning circuit draw 16mA (with \( f_c=20MHz \)) from 3.3 V supply, and occupy an area of 0.45 mm\(^2\).

1. Introduction

Most modem direct broadcast satellite (DBS) tuners use direct conversion architecture to minimize complexity and power. In a direct conversion DBS tuner (Fig.1), I/Q broadband mixers down-convert a cluster of channels from the L-band (950MHz-2150MHz) directly to baseband. The baseband I/Q LPFs select the desired channel signal, which is then converted to digital bits through ADCs in the digital demodulator chip for further processing.

![Fig.1. A DBS Tuner front end](image)

The baseband LPF has to meet strict specification from system requirements:

1. Moderate passband ripple, sharp transition band, large stopband attenuation, moderate group delay ripple. Since the DBS channel date rate can vary from 1 to 45Mps, the cutoff frequency of the channel selection LPF should be tunable from 4MHz to 40MHz to cut off the closely spaced unwanted neighbor channel interferences. An automatic tuning system is needed to maintain the precise filtering characteristics against process variation, temperature drift and aging.
2. Since there is no filtering until the baseband LPF, the LPF itself should be very linear. Fortunately, satellite links are directional point-to-point communications that do not suffer from strong multi-path interference, as is the case for terrestrial and mobile TV applications. So for DBS tuners, the blocker signals can be only 20 dB stronger than the desired channel (considering worst case spectrum tilt and channel to channel receive power variation)[1]. From this point of view, the filter should have enough signal-handling capacity. In terms of figure of merit, the I-dB compression point \( V_{ip3} \) is more useful to assess the linear performance of the filter than the third-harmonic intercept voltage \( V_{ip3} \).
3. System simulations indicate that a baseband VGA should be placed in front of the LPF to optimal noise and linearity line-up. So the noise specification of the LPF is not so challenge and can be compromised for lower power consumption.

The paper is organized as follows. In section II, the filter topology and the automatic tuning system are described at the system level. Section III discusses the circuit design of the building blocks. Simulation results are given in section IV and section V contains the conclusions.

2. System design considerations

2.1 About the main filter topology

For the main filter, a 7th-order Butterworth leapfrog Gm-C filter topology is selected based on the following observations:

1. A leapfrog realization of a low pass filter has lower sensitivities of the passband frequency response to individual element values than a cascaded biquads realization[2].
2. The Gm-C topology is usually preferred at high frequency for its lower power consumption relative to active-RC or MOSFET-C structures.
3. If implemented in bipolar or BiCMOS technology, the Gm cells can be accurate tuned through bias current variation as they depend directly on a linear gm-Ic relationship, the fundamental translinear behavior of the bipolar junction transistor. As a result, Gm-C filter’s cutoff frequency, which is proportional to Gm/C, can have a wide tuning range.

Here, we use the bipolar junction transistor in our 0.35um SiGe BiCMOS technology to design a novel translinear Gm cell which has a large enough signal-handling capacity and moderate low noise. By proper bias circuits design, the cutoff frequency of the implemented Gm-C main filter can also be directly proportional to a control current. In other words, we have a linear tunable ICF (current controlled filter.)

2.2 About corner frequency programmability and on chip automatic tuning

System specifications requires that the -3dB cutoff frequency \( f_c \) of the LPF can be digital programmed from 4MHz to 40MHz and the switching step should be as fine as possible to cut off the closely spaced unwanted neighbor channel interferences. Already having a linear tunable current controlled main filter, we can use a linear current DAC to achieve digital programmability with a fine step. The output current of the DAC responding to the input digital bits is then used to control the main filter, thus the cutoff frequency of the main filter can be programmed within the DAC’s resolution. Here a 7-bit linear current DAC is implemented.

978-1-4244-2186-2/08/$25.00 ©2008 IEEE

Authorized licensed use limited to: INSTITUTE OF SEMICONDUCTORS CAS. Downloaded on November 25, 2009 at 01:31 from IEEE Xplore. Restrictions apply.
To guarantee accurate and stable filtering characteristic, on-chip automatic frequency tuning is needed. In the proposed design, a master-slave tuning system locks the main filter’s frequency response to a reference clock signal. The PLL-based on chip automatic tuning system is shown in Fig.2.

Fig.2. The filter system block diagram

The 5-bit R counter divides the tuner system crystal frequency by R. The frequency-divided clock signal feeds a second-order linear tunable ICF, which is a fully differential Gm-C low pass biquad (see Fig.7). The phase detector compares the phase difference between the input and output of the ICF and changes the pole frequency of the ICF through a control current until the output is in quadrature with the input. Then the pole frequency of the ICF is equal to the reference frequency, which means that controlled by this current, the biquad ICF now exhibits an accurate and stable frequency response. Since the Gm-C biquad ICF use the same Gm cell topology as the main filter, and the capacitors used in the ICF and those in the main filter can be matched very well, the control current of the biquad ICF can also be used to derive that of the main filter to maintain a stable main filter frequency response. Here we “properly” scale it (see Fig.2) and use its two scaled versions as the two reference currents for the 7-bit linear current DAC. The DAC is designed to have the property that when its digital input is all “0”s, its output is its lower reference current, and when its digital input is all “1”s, its output is its higher reference current. In this way, we can fine tune the main filter’s cutoff frequency through the 7-bit DAC without relocking the PLL, which means a very small tuning time. A relatively longer tuning time is needed when we have to change R to achieve a coarse tuning by relocking the PLL to a new reference frequency.

3. Circuit design

3.1 Gm cell

The Gm cell design is most critical for the whole filter and tuning system design. The Gm cells designed should have large enough linear input range, reasonable low noise and wide bandwidth. They should be easily tunable and low power consumption. The DBS tuner in which the LPF is embedded adapts a 3.3-V supply voltage. So the Gm cell should be able to operate with 3.3-V supply voltage under all operating conditions.

The Gm cell used in the main filter and the biquad ICF is a modified multitanh doublet[3]. Fig.3(a) shows a standard multitanh doublet Gm cell, which has a small-signal transconductance of \( G_m = \frac{8I_1}{25V_T} \) (where \( V_T \) is the thermal voltage,) 36 percent smaller than that of a simple bipolar differential pair biased with the same total tail current. As a result of this linearization technique, this Gm cell has a much wider input range (96mv peak-to-peak differential ppd) than that of a simple differential pair (32mvppd) beyond which the total harmonic distortion (THD) of the output current becomes greater than 1 percent (-40dB). In order to further extend the linear input range, an “emitter-degenerated” multitanh doublet can be used as the filter’s Gm cells (Fig.3(b))\[4\]. Diode connected bipolar transistors instead of normal resistors are used as the degeneration resistors in order to maintain the linear gm-IC relationship of the standard multitanh doublet. This Gm cell supports an input signal of about 200 mVppd for better than -40dB THD. However, the “emitter-degenerated” multitanh doublet Gm cell is only suitable for operation with 5-V supply voltage and runs out of headroom for 3.3-V supply voltage under the worst case operating conditions. In order to design a translinear Gm cell that can be operating with 3.3-V supply voltage and have large enough linear input range, we can fold the diodes to save the precious voltage headroom(Fig.3(c)). The “folded” multitanh doublet Gm cell has a signal capacity of 300mVppd for better than -40dB THD. Fig.4 shows the simulated plot of Gm-versus input signal for the standard, the emitter-degenerated and the folded multitanh doublet Gm cells, which are biased with the same total tail currents. As in the standard multitanh doublet and a simple differential pair case, here the value of transconductance is again traded for larger linear input range.

Fig.3 (a) A standard multitanh doublet Gm cell. (b) An “emitter-degenerated” multitanh doublet Gm cell. (c)A folded “emitter degenerated” multitanh doublet Gm cell.
3.2 Main filter
The structure and the component values of the 7th-order Butterworth leapfrog Gm-C filter are derived from the double terminated LC ladder LPF prototype by signal flow graph transformation. In cases where the output currents of several Gm cells are combined, we need one load circuit only. So in practice we need half as many load circuits as the Gm cell input stages[5]. The resulted topology is drawn in Fig.5. Node scaling is performed by properly scale the individual Gms to optimize the dynamic range of the filter and to compensate for the inherent 6 dB loss of the LC prototype. The integrating capacitors are split as anti-parallel ones to keep the back-plate parasitic capacitances balance to the n/p signal lines. Values of the actual capacitors are modified by deducing that of CMFB compensating capacitors and the parasitic capacitances contributed by the Gm cells. The main filter’s bias cell is shown in Fig.6. The control current is mirrored to the tail currents of the Gm cells with different scaling ratios based on their individual Gm values. Voltage routing techniques is used to improve the matching between the Gm cells, which requires a careful layout floor planning to properly route the base voltage bias line \( V_{tune} \).

3.3 the biquad ICF
The ICF in the tuning circuit is a classic fully differential biquad with low-pass output (Fig.7). The low-pass transfer functions are

\[
H(s) = \frac{G_{m1}G_{m2}}{s^2C_1C_2 + sC_2G_{m1} + G_{m1}G_{m2}}
\]  

(1)

The pole frequency \( \omega_0 \), the filter quality factor Q and the gain at the pole frequency of the biquad are

\[
\omega_0 = \sqrt{\frac{G_{m1}G_{m2}}{C_1C_2}}
\]

\[
Q = \sqrt{\frac{G_{m1}}{G_{m2}}} \frac{C_2}{C_1}
\]

\[
H(s) \big|_{s=j\omega_0} = \frac{QG_{m1}}{jG_{m2}}
\]

(2)

The pole frequency, the output of the ICF is in quadrature to its input. The proper functioning of the PLL requires us to choose \( G_{m1}=0.5G_{m2} \) to make a moderate \( Q=8.4 \). The ICF’s bias cell is identical to that of the main filter in topology.

3.4 the DAC
The 7-bit DAC is a current-steering type linear DAC. Its concept schematic is shown in Fig.8. IDACH and IDACI are the DAC’s high and low reference current, respectively. When the DAC’s input is swept from all Os to all 1s, its output current will vary linearly from IDACI to IDACh. Since the DAC is out of the PLL loop, it should be carefully designed to make its transfer characteristic independent of process variation and temperature drift, which is possible because the characteristic of the DAC depends only on elements matching. So a careful layout is also important here.
Simulation results are summarized in Table I. And a comparison is made with the measurement results of the filter from [4] which uses the “emitter-degenerated” $g_m$ cells in the main filter and the ICF.

<table>
<thead>
<tr>
<th>Work</th>
<th>This work</th>
<th>Work in [4]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.35 um SiGe BiCMOS</td>
<td>7th-order Butterworth LPF</td>
</tr>
<tr>
<td>Filter type</td>
<td>4MHz to 40MHz</td>
<td></td>
</tr>
<tr>
<td>Supply voltage</td>
<td>3.3 V</td>
<td>5 V</td>
</tr>
<tr>
<td>Filter’s input referred noise ($f_o = 20$MHz)</td>
<td>28nV / $\sqrt{Hz}$</td>
<td>30nV / $\sqrt{Hz}$</td>
</tr>
<tr>
<td>Filter’s passband IIP3 ($f_o = 20$MHz, $f_{signal} = 10$MHz, 11MHz)</td>
<td>-2dBVrms</td>
<td>-3dBVrms</td>
</tr>
<tr>
<td>Filter’s stopband IIP3 ($f_o = 20$MHz, $f_{signal} = 30$MHz, 45MHz)</td>
<td>24dBVrms</td>
<td>27dBVrms</td>
</tr>
<tr>
<td>Filter’s $V_{1dB}$ ($f_{signal} = 10$MHz)</td>
<td>303mV</td>
<td>208mV</td>
</tr>
<tr>
<td>Current consumption (I/Q filters + tuning circuits $f_o = 20$MHz)</td>
<td>16mA</td>
<td>13mA</td>
</tr>
<tr>
<td>Die size (I/Q filters + tuning circuits)</td>
<td>0.45mm$^2$</td>
<td>0.5mm$^2$</td>
</tr>
</tbody>
</table>

5. Conclusion

A high frequency and widely tunable continuous-time low pass filter has been implemented in a 0.35um SiGe BiCMOS technology. A novel on chip automatic tuning scheme has been successfully realized. The simulation results show that the filter system is well suited for a direct conversion DBS tuner.

Acknowledgements

The authors wish to thank Xueqing Hu, Ming Gu and Peng Yu for their encouragement and test support. Thanks also to Juan He for help in layout.

References