The influence of low-temperature Ge seed layer on growth of high-quality Ge epilayer on Si(1 0 0) by ultrahigh vacuum chemical vapor deposition

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Abstract

High-quality Ge epilayer on Si(1 0 0) substrate with an inserted low-temperature Ge seed layer and a thin Si0.77Ge0.23 layer was grown by ultrahigh vacuum chemical vapor deposition. The epitaxial Ge layer with surface root-mean-square roughness of 0.7 nm and threading dislocation density of $5 \times 10^5$ cm$^{-2}$ was obtained. The influence of low temperature Ge seed layer on the quality of Ge epilayer was investigated. We demonstrated that the relatively higher temperature (350°C) for the growth of Ge seed layer significantly improved the crystal quality and the Hall hole mobility of the Ge epilayer.

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1. Introduction

The growth of high-quality strain-relaxed thick germanium epilayer with smooth surface, low defect density, and thin buffer layers on silicon substrates has attracted great attention due to its compatibility with Si process technology and the application in photonic and electronic devices. Germanium epilayers on Si substrates can be used for fabrication of high-performance Si-based Ge photodetectors operating at long wavelength of 1.3–1.55 μm [1], high-mobility metal-oxide-semiconductor field-effect transistors (MOSFETs) [2], or the platform for the integration of III–V optoelectronic devices on Si [3].

The main challenge of epitaxy Ge on Si substrate is 4.18% lattice mismatch between Ge and Si, which can cause rough surface and high defect density. Several methods have been exploited to grow high-quality Ge film on Si substrate, such as those using compositionally graded buffer layer [4,5], two thin SiGe buffer layers [6], surfactant-mediated epitaxy [7], selective area growth [8], and low temperature (LT) and high temperature (HT) two-step growth approach combined with thermal annealing [9,10]. However, the graded SiGe buffer layers are required to be about 10 μm thickness with Ge composition ranging from 0 to 1, which is not appropriate for monolithic integration of devices on Si and has poor thermal conduction. In order to reduce the buffer layer’s thickness, double thin SiGe layers utilizing interface blocking and in situ annealing has been reported [6]. Ge epilayer with a threading dislocation density (TDD) of $3 \times 10^5$ cm$^{-2}$ and root-mean-square (RMS) surface roughness of 3.2 nm was achieved [6]. The total thickness of the double thin SiGe buffer layers is about 1.6 μm, which is still too thick for practical integration. For the LT and HT two-step growth
approach, the first step is the deposition of ultra thin (30–50 nm) Ge seed layer on Si at LT of 300–400 °C to relieve the misfit stress and maintain a smooth surface, using limited mobility of Ge adatoms and surfactant action of H to prevent commonly SK growth mode [11,12], and the second step is growing thick Ge layer at HT of 600 °C for faster growth rate and higher crystal quality, followed by thermal annealing [9,10]. The surface of the Ge film obtained through this method is rather smooth and the RMS value is less than 1 nm, but TDD is extremely high, close to $1 \times 10^{8} \text{cm}^{2}$ [9,10]. Thermal annealing is indispensible included to reduce the TDD to the acceptable value. To decrease TDD from $9 \times 10^{6}$ to $2 \times 10^{6} \text{cm}^{2}$, 10 cycles of thermal annealing was ex situ performed [9]. Recently, Nakatsuru et al. [13] and Loh et al. [14] reported a modified two-step growth approach, i.e., growing an ultra thin (2–30 nm) LT SiGe buffer layer prior to the deposition of LT Ge seed layer and HT Ge layer. With the help of LT SiGe layer to absorb partially misfit strain, provide Ge nucleation sites, and coalesce dislocations, the TDD can be reduced to $6 \times 10^{6} \text{cm}^{2}$, without any thermal annealing.

In Refs. [13,14], the influence of Ge content, thickness, and growth temperature of SiGe buffer layer on the quality of epitaxial Ge films were investigated. In this work, high-quality Ge epilayer on Si utilizing modified two-step approach by ultrahigh vacuum chemical vapor deposition (UHVCVD) was achieved with a surface RMS roughness of less than 1 nm and a TDD of $5 \times 10^{6} \text{cm}^{2}$. The impact of LT Ge seed layer on the quality of the HT Ge epilayer was studied. It is shown that Ge epilayer grown on the relatively higher temperature Ge seed layer has a superior quality as demonstrated in (a) lower TDD, (b) smaller full-width at half-maximum (FWMH) of X-ray diffraction (XRD) profiles, and (c) higher hall hole mobility at room temperature.

2. Experiments

Two samples were grown by UHVCVD system with a base pressure of $5 \times 10^{-8} \text{Pa}$. Pure Si$_2$H$_6$ and GeH$_4$ were used as precursors. The growth processes were in situ monitored by reflection high-energy electron diffraction (RHEED). The substrates were 4 in p-type Si (100) wafers with resistivity in the range of 12–18 Ωcm. The wafers were cleaned by RCA method and dried by N$_2$ before loading into the growth chamber. Firstly, the wafer was baking at 850 °C for 30 min to de-oxide, followed by Si buffer growing at 750 °C to obtain a clean epi-ready surface. Then 50 nm Si$_{0.77}$Ge$_{0.23}$ buffer layer was grown at 450 °C with a growth rate of about 0.58 nm/min. After that, LT Ge seed layer was grown at 330 °C for sample A and 350 °C for sample B. Finally, 300 nm HT Ge top layer was grown at 600 °C with a growth rate of 1.17 nm/min. The duration of deposition of the Ge seed layer was 4 h for both samples and the thickness was about 40 nm for sample A and 50 nm for sample B, respectively. The total pressure during growth was about $2 \times 10^{-2} \text{Pa}$. There was no need of Si$_2$H$_6$ for the growth of LT Ge and HT Ge, and for the growth of SiGe, the ratio of flow rates of Si$_2$H$_6$ to GeH$_4$ was about 1:1.

The strain status and crystal quality of Ge layers were evaluated by double crystal XRD measurement (Bede, D1 system), using a Cu K$_{\alpha1}$ ($\lambda = 0.15406$ nm) as the X-ray source, and Raman scattering (Renishaw, UV–Vis Raman System 1000), using Ar$^+$ laser ($\lambda = 514.5$ nm). The TDD was measured by etch pit density (EPD) counting. The pits were formed from selectively chemical etching by a solution of HF, HNO$_3$, CH$_3$COOH, and I$_2$ [9]. The surface morphology was analyzed by atomic force microscopy (AFM, Seiku Instruments, SPI4000/SPA-400) in a tapping mode. Hall measurement was carried out on HL55WIN Hall System at room temperature.

3. Results and discussion

3.1. RHEED patterns

Typical RHEED patterns during growth are shown in Fig. 1. Figs. 1(a) and (c) are related to the LT Ge seed layers, and (b) and (d) are related to the HT Ge layers. During the deposition of SiGe buffer layer, the $\frac{1}{2}$ streaks are clearly observed and a flat surface for both of the samples are suggested. After the growth of Ge seed layer at 330 °C (Fig. 1(a)), the RHEED pattern shows weak $\frac{1}{2}$ streaks, indicating a slightly wavy surface. Along with the deposition of HT Ge layer, the Ge surface evolves towards a smoother surface and finally a well developed $2 \times 1$ reconstruction can be observed (Fig. 1(b)). In comparison, Ge seed layer grown at 350 °C develops a rough surface as the $\frac{1}{2}$ streaks disappear and spots come out along $1 \times 1$ streaks (Fig. 1(c)). The temperature of 350 °C is not low enough to prohibit three-dimensional growth [18], and the surface becomes much rough. However, after deposition of HT Ge layer, the surface becomes smooth and $2 \times 1$ reconstruction is rebuilt (Fig. 1(d)).

3.2. XRD and Raman measurements

The $\Omega–20$ symmetric (0 0 4) XRD scans of Ge epilayers are shown in Fig. 2, including bulk Ge (0 0 4) peak position expected from theory. For each curve, three peaks originating from Si substrate, SiGe buffer layer, and Ge epilayer are clearly visible. Note that the line shapes are very symmetric for both of the Ge peaks, implying that the strain relaxation is homogeneous. The peak distance between Ge epilayer and Si is 5530 and 5474 arcsec for Ge seed layer grown at 330 °C (sample A) and 350 °C (sample B), respectively. These two values are smaller than the expected one between the fully relaxed Ge and Si. According to Bragg’s law with $\lambda = 0.15406$ nm for Cu K$_{\alpha1}$ radiation, the peak distance is 5649 arcsec with the relaxed lattice constants 0.5431 and 0.5658 nm for Si and Ge. The smaller peak distance between epitaxial Ge and Si substrate
indicates that the epitaxial Ge layer is under tensile strain. From the peak positions, the in-plane lattice constant is evaluated to be 0.5664 nm for sample A, corresponding to the in-plane tensile strain of 0.12%. For sample B, the strain is calculated to be 0.17%, which is bigger than that of sample A. The FWHM of Ge peak for sample A is much wider than that of sample B, implying the higher TDD in the sample A.

Raman spectra were also measured to evaluate the crystalline quality and in-plane strain in Ge layers. As shown in Fig. 3, solid lines are experimental data and dashed lines are from Lorentzian fit. Also indicated is Ge–Ge mode from bulk Ge as dotted straight line in the figure. The peaks locating at around 300 cm$^{-1}$ are from Ge–Ge mode of Ge layers. The peak position is 300.5 cm$^{-1}$ for sample A and 299.8 cm$^{-1}$ for sample B, respectively. The value of in-plane strain can be estimated by using empirical expression [15]

$$\omega (\text{cm}^{-1}) = 300.8 - 400\varepsilon_1,$$

where $\omega$ is Raman shift of Ge–Ge mode and $\varepsilon_1$ is the in-plane strain in Ge epilayer. The stain for sample A is 0.08%, which is smaller than that for sample B (0.25%). The magnitude of strain is very similar to that evaluated from XRD data. XRD and Raman spectroscopy suggest that sample B has a higher residual tensile strain. The FWHM for the two Ge–Ge mode peaks are much small,
in the order of 6 cm\(^{-1}\), suggesting that the quality of top Ge layers is quite good.

### 3.3. Surface roughness and dislocations

Surface morphology of Ge layers was examined with the help of AFM. Typical 10 \(\times\) 10 \(\mu\)m\(^2\) AFM images of Ge layer are shown in Fig. 4. Analysis of these AFM images indicates smooth surface with low RMS roughness of 0.6 nm for Ge layer on Ge seed layer grown at 330 °C (sample A) and 0.7 nm of that at 350 °C (sample B). It is interesting to note that no typical cross-hatch surface pattern, usually observed with thick SiGe layers grown on Si(1 0 0) substrates, is visible in these samples. Cross-hatches are typically associated with variation of strain across the surface. Their absence is another good feature of the studied samples. For our Ge epilayers, the RMS roughness is less than 1 nm, which is much smoother than that of Ge layer grown on graded buffer layers [5].

TDDs were measured by counting pits formed from selectively chemical etching with the help of Nomarski optical microscope. For each sample, more than 10 images were taken and the values were averaged to get a statistically accurate numbers. The TDDs for sample A and sample B are 2 \(\times\) 10\(^6\) and 5 \(\times\) 10\(^5\) cm\(^{-2}\), respectively. TDD is relatively higher in sample A, but still significantly lower than that without LT SiGe buffer layer [9,10].

### 3.4. Hall hole mobility

Hall effect measurements were carried out at room temperature. The results show that the Ge layers are p-type with hole mobility of 290 and 550 cm\(^2\)/V/s for Ge seed layer grown at 330 °C (sample A) and 350 °C (sample B), respectively. This is closely associated with the structural defects in the Ge layers, which leads to acceptor states near the valance band edge [16]. The relatively higher mobility of sample B indicates that its defect density is much lower, in accordance to the EPD results.

### 3.5. Discussion

From analysis of XRD and Raman measurements, the Ge epilayers are under tensile strain. The phenomenon that Ge layer is in a tensile strain configuration was also confirmed by other groups [1,7,10]. The tensile strain in Ge epilayer is induced by thermal expansion coefficient
mismatch between Si and Ge during cooling process from elevated growth or annealing temperature to room temperature.

The strain in Ge layer can be divided into two parts: (1) compressive strain due to the lattice mismatch between Si and Ge, and (2) tensile strain induced by the cooling process because of the thermal expansion coefficient mismatch. For the HT Ge layers on Ge seed layers grown at 330 °C (sample A) and 350 °C (sample B), the tensile strain for the cooling process are the same (from 600 °C to room temperature), so the tensile strain induced in these Ge layers are the same, i.e., 0.19% predicted by the theoretical calculations [17], which is very close to the experimental data. The residual compressive strain before cooling should take the responsibility for the different amount of final tensile strain in Ge layers. The tensile strain in Ge epilayer on Ge seed layer grown at 350 °C (sample B) is larger, indicating smaller or no residual compressive strain in the Ge seed layer. The relatively higher growth temperature for the Ge seed layer is of great benefit for strain relaxation.

Although Ge seed layers of samples A and B are much thicker than the equilibrium critical thickness (1–2 nm), the degree of strain relaxation of Ge seed layer is no more than 90% (also see Refs. [10,13,14,18]). It is suggested that it is very difficult to fully relieve the strain in the Ge seed layer when growing at LT (300–400 °C). This is because of the erosion of the interface caused by vacancies [19], and high nucleation barrier for misfit dislocations (MDs) when surface roughening is forbidden [20,21]. LeGoues et al. [21] have reported that As-mediated Ge layer grown on Si with thickness about 10 monolayers (ML) can remain pseudomorphically strained. The other part of relaxation takes place during the process of Ge thick layer growth at HT.

From the variation of RHEED patterns, we note that the higher temperature for the growth of Ge seed layer, the rougher of the surface. Surface roughness can lead to large local stresses at islands or pits edge, and hence dramatically reduce nucleation barrier of MDs [22–24]. The strain is easily relieved by formation of MDs for a rough surface. So the degree of relaxation for the Ge seed layer grown at 350 °C is higher; and also, with a higher growth temperature, the dislocation glide velocity is faster [25], resulting in lower TDDs.

For Ge films grown by modified two-step approach, extremely lower TDDs were obtained in comparison with those grown without SiGe buffer layer [9,10], which is due to the impact of SiGe buffer layer prior to the deposition of LT Ge. As that has been systemically investigated by Nakatsuru et al. [13] and Loh et al. [14], SiGe buffer layer is employed to provide LT Ge nucleation sites, coalesce and annihilate dislocations, and absorb partially strain energy from mismatch of Ge to Si. With the help of SiGe buffer layer, Ge films have much lower TDD values and no thermal annealing is required.

4. Conclusion

We have grown high-quality Ge on LT Ge seed layer in combination with LT SiGe buffer layer by UHVCVD. It is shown that the Ge surface is much smooth, with RMS roughness of less than 1 nm and the TDD is much low, in the order of 10^6 cm^-2, without any thermal annealing. It is also demonstrated that the Ge layer on the Ge seed layer grown at the relatively higher temperature has improved quality with lower TDD and higher hole mobility.

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