A Low-Power Column-Parallel ADC for High-Speed CMOS Image Sensor

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ABSTRACT

This paper presents a 10-bit low-power column-parallel cyclic analog-to-digital converter (ADC) used for high-speed CMOS image sensor (CIS). An opamp sharing technique is used to save power and area. Correlated double sampling (CDS) circuit and programmable gain amplifier (PGA) are integrated in the ADC, which avoids stand-alone circuit blocks. An offset cancellation technique is also introduced, which reduces the column fixed-pattern noise (FPN) effectively. One single channel ADC with an area less than 0.03mm² was implemented in a 0.18μm 1P4M CMOS image sensor process. The resolution of the proposed ADC is 10-bit, and the conversion rate is 2MS/s. The measured differential nonlinearity (DNL) and integral nonlinearity (INL) are 0.62 LSB and 2.1 LSB together with CDS, respectively. The power consumption from 1.8V supply is only 0.36mW.

Key words: CMOS image sensor, column-parallel cyclic ADC, correlated double sampling, offset cancellation

1. INTRODUCTION

High-speed CMOS image sensors (CIS) are widely used in motion capture, crash test, machine vision and scientific research. Except for the high-speed pixels, fast and accurate readout circuits are also essential in these applications. In fact, a high-speed high-resolution analog-to-digital converter (ADC) is one of the most critical building blocks in the readout signal chain. Trading off among the area, power, resolution and speed requirements, column-parallel ADC array has been proven to be one of the best choices [1].

Some column-parallel ADC converters for high speed image sensor have been reported [2]. Single-slope ADC is simple and small, but its speed is usually insufficient when the frame rate of the sensor is extremely high. Successive-approximation (SAR) ADC has also been used in many image sensors [3] [4]. Unfortunately, SAR ADC requires a high-precision internal digital-to-analog converter, and it is difficult to achieve 10-bit or more resolution at the column of the CMOS image sensors. ΣΔ ADC might be adopted as well [5]. However, while its resolution is high enough, the speed and power consumption are unable to meet the requirements when integrated in one column. Cyclic or algorithmic ADC is another alternative. It has moderate conversion rate and resolution. The linearity of the cyclic ADC is the best due to its inherent operating principle. When properly designed, the area and power consumption can be reduced to a very low level. There are many CIS sensors that employ the cyclic architecture as well [6] [7]. However, the area of the implemented ADC is quite large [8]. This requires the pixel to be large enough to fit the width of ADC, which increases the total area of the chip. The oversized pixel also makes it difficult to realize a large pixel array or achieve high
resolution.

This paper presents a 10-bit column-parallel cyclic ADC with correlated double sampling (CDS) and programmable gain amplifier (PGA) for high-speed CMOS image sensors. The column-parallel cyclic ADC circuit has the following advantages: 1) CDS circuit is integrated in the ADC and performed at the starting phase of conversion. This greatly saves chip area instead of realizing an independent CDS circuit; 2) PGA circuit is implemented at the same time so that the analog output signal of the pixel can be adjusted to meet the full-scale of the column-parallel cyclic ADC circuit; 3) an opamp sharing technique is used to further reduce the total power and area; 4) a novel offset cancellation technique is adopted to reduce opamp’s offset and column fixed-pattern noise (FPN). Owing to the embedded CDS, embedded PGA, opamp sharing and offset cancellation technique, the area of one single channel ADC is greatly reduced and less than 0.03mm².

2. ARCHITECTURE

Fig.1 shows the block diagram of the high speed CIS. It is mainly composed of a pixel array, two ADC sub-arrays, and a digital controller. A classical 4T pixel \cite{9,10} structure is used for the pixel. The ADC sub-arrays are placed at upper and lower sides of the pixel array and simultaneously convert the analog output signals of the pixels in even columns and odd columns, respectively. The digital controller generates the key control signal of pixels and ADCs. It also performs a parallel-to-serial conversion and buffering of the output digital codes coming from the ADC arrays.

![Fig. 1 Block diagram of the CIS.](image1)

![Fig. 2 Concept of opamp sharing.](image2)

The 10-bit column-parallel cyclic ADC consists of four main building blocks: a track and hold amplifier (THA), a quantizer (sub-ADC), a multiplying digital-to-analog converter (MDAC), and a digital error correction block (DEC). The THA is used to sample and hold the input signal and shift it to an appropriate voltage level. It performs the CDS operation at the same time. With the digital control word properly set, the THA can also be considered as a PGA. The high-performance opamp in the THA is shared with that in the MDAC, which greatly increases the hardware efficiency. The concept is shown in Fig. 2. The quantizer is composed of comparators and digital decoding circuits. It is essentially a 1.5bit flash ADC which converts the voltage signal from analog domain to digital domain. The MDAC mainly comprises of op-amp and switched-capacitors. It performs the following three operations: subtraction, multiplication and...
digital-to-analog conversion. Output value of the sub-ADC determines the reference voltage to be subtracted from the input. The residue voltage is then multiplied by 2 and sent back to the quantizer for usage of the next period. DEC is a digital circuit block. It is used to perform the error correction and to synchronize the output digital code. The block diagram of the ADC is shown in Fig. 3.

![Block diagram of the cyclic ADC](image)

Fig. 3 Block diagram of the cyclic ADC.

$V_{rst}$ and $V_{sig}$ are the pixel output reset and signal voltages, respectively. The THA samples them at first and performs CDS operation at the same time to reduce pixel FPN. According to the control bits, a gain may be achieved simultaneously. In the next step, sub-ADC works first to determine the subtraction threshold in the non-overlapping time. Based on the output of sub-ADC, MDAC settles in the remaining time, and completes the subtraction and multiplication operations. The operations of the subsequent five cycles are similar, which means 10 bits can be resolved in total. At the end of the last clock period, DEC corrects the error and synchronizes the output digital code. Same as the pipelined ADC, a 1.5bit structure is used for sub-ADC and MDAC. This scheme increases the comparator offset tolerance to $\pm Vr/4$ and is most hardware efficient. Clock generator block is integrated on chip and is configurable through a serial interface to adjust the working parameters of the sensor. The analog references for comparators and op-amps are supplied by off-chip circuits.

3. **CIRCUIT DESIGN**

Since MDAC is the most critical and complex part of the ADC, we mainly describe the design of the MDAC here. Fig. 4 shows the schematic of the MDAC. Its core component is a fully-differential high-gain switched-capacitor amplifier, which is shared with the THA. The corresponding timing chart is shown in Fig. 5.
The whole operating procedure can be divided into two phases: noise canceling phase and ADC converting phase. Fig. 6 depicts the equivalent circuits of the noise canceling phase. This phase is made up of two steps: Step A and Step B. In Step A, $V_{rst}$ and the positive reference $V_{rp}$ are connected to the bottom plates of $C_{SP}$ and $C_{SN}$, respectively. Capacitors $C_1$, $C_2$, $C_4$, $C_5$ are short-circuited to clear the charge on them. The opamp is configured in a unity-gain feedback mode with $C_3$ and $C_6$ cross-connected between its input and output. As illustrated in Fig. 6(a), this configuration reversely stores opamp’s offset $V_{os}$ on $C_3$ and $C_6$, and makes its influence negligible after the cyclic ADC conversion.

In Step B, depicted in Fig. 6(b), $V_{sig}$ and the negative reference $V_{rn}$ are connected to $C_{SP}$ and $C_{SN}$ respectively. $C_3$ and $C_6$ are acting as the feedback capacitors this time while $C_1$ and $C_4$ sampling the opamp’s output. It results in the $V_{sig}$ being subtracted from $V_{rst}$, accomplishing correlated double sampling to remove threshold mismatches between pixels [1].

In order to fit ADC’s full scale range, which is designed to be $\pm 1V$, a $\times 2$ operation as well as a level-shift is performed at the same time. This is achieved by making $C_{SP} = C_{SN} = 2C_3 = 2C_6$ and properly choosing the reference voltages. After all of the above operations, that is, at the end of the noise canceling phase, the differential output voltage $V_{out}(0)$ is given by:

$$V_{out}(0) = V_{op} - V_{on} = 2(V_{rst} - V_{sig}) - 2(V_{rp} - V_{rn}) - V_{os}$$

(1)

When $\Phi_S$ changes to zero, the ADC enters into the cyclic converting phase. In this stage, two sets of capacitors are used to sample the output of the amplifier and transfer the charge, which will double the readout speed. A two-phase
non-overlapping clock is generated to form the required control signals, i.e. $\Phi_1$ ($\Phi_1'$, $\Phi_1''$) and $\Phi_2$ ($\Phi_2'$, $\Phi_2''$). In each of the non-overlapping time, comparators of the sub-ADC work and produce one of the three digital codes: \{00, 01, 10\}. This code is subsequently used to determine which reference voltage will be connected to the input capacitors, which will realize the 1.5bit algorithm. The subtraction, multiplication and digital-to-analog conversion are done by MDAC according to the results of the sub-ADC. Or it can be expressed in equation (2):

$$V_o = \begin{cases} 
2V_t + V_r & (b = 0) \\
2V_t & (b = 1) \\
2V_t - V_r & (b = 2) 
\end{cases}$$

(2)

An important advantage of the 1.5-bit algorithm is its tolerance on comparator offset. Up to $\pm V_r/4$ offset can be corrected in the digital domain [11]. This margin enables the comparator to be designed with a relatively simple structure, greatly reducing its area and power dissipation.

In the odd phase, the bottom plates of $C_1$ and $C_4$ are connected to the amplifier’s output, while their top plates are connected together. They serve as the sampling capacitors in this phase when the opamp is settling. The top plates of $C_2$ and $C_5$ are connected to the summing nodes, with their bottom plates connected to references determined by the sub-ADC. In the even phase, the roles of the input capacitors ($C_2$ and $C_5$) and the sampling capacitors ($C_1$ and $C_4$) are exchanged, and the same operation is performed. This results in 1.5bit output codes being resolved on both rising and falling edges of the clock, so that a 10bit resolution can be obtained in only five cycles. The equivalent circuits of the two phases are shown in Fig. 7.

As the ADC switching between the odd and even phases, the following relationship holds:

$$V_{out}(i + 1) = 2V_{out}(i) - b(i) \times V_r + V_{os}$$

(3)

Since $V_{out}(0)$ expressed in equation (1) has the $-V_{os}$ term intentionally introduced, it can be found that the opamp’s offset voltage doesn’t accumulate after arbitrary cycles, and the final error voltage is still $-V_{os}$. Assuming N is the resolution of the ADC, which is 10 in this design, the input-referred offset can be calculated as:

$$V_{os^*} = \frac{-V_{os}}{2^{N-1}} \approx 0$$

(4)

Whereas without the offset cancellation, this would be:

$$V_{os^*} = \frac{V_{os}(1+2^2+2^3+\ldots+2^{N-1})}{2^{N-1}} \approx 2V_{os}$$

(5)

Equation (4) suggests that the offset cancellation technique can lower the column fixed-pattern noise induced by opamp’s offset to a negligible level.
4. EXPERIMENTAL RESULTS

The proposed ADC is fabricated in a 0.18μm 1P4M CIS process. A pixel array is integrated with two column-parallel ADC sub-arrays to implement a high-speed CMOS image sensor. In the ADC testing mode, a sine wave input is provided by signal generator as the signal voltage \( V_{\text{sig}} \), and a fixed dc potential is supplied by on-board regulator to emulate the reset voltage \( V_{\text{rst}} \). Fig. 8 shows the measured DNL and INL:

![DNL and INL plots](image)

As can be seen, the DNL is \(+0.28 / -0.62\) LSB, and the INL is \(+2.1 / -2.1\) LSB. Note that the performance not only characterizes the ADC itself, but also with the built-in noise canceller. Table 1 summarizes the ADC performance results.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Ref. [6]</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
<td>0.25μm CMOS 1P4M</td>
<td>0.18μm CMOS 1P4M</td>
</tr>
<tr>
<td>Resolution</td>
<td>12 Bit</td>
<td>10 Bit</td>
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<tr>
<td>Sample rate</td>
<td>2MS/s</td>
<td>2MS/s</td>
</tr>
<tr>
<td>Input range</td>
<td>2Vpp</td>
<td>2Vpp</td>
</tr>
<tr>
<td>DNL</td>
<td>+0.76 / -0.81 LSB</td>
<td>+0.28 / -0.62 LSB</td>
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<tr>
<td>INL</td>
<td>+20.6 / -2.25 LSB</td>
<td>+2.1 / -2.1 LSB</td>
</tr>
<tr>
<td>Size</td>
<td>40μm×2200μm</td>
<td>20μm×1400μm</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>130 μA @3.3V</td>
<td>200 μA @1.8V</td>
</tr>
</tbody>
</table>
5. CONCLUSION

A 10-bit column-parallel cyclic ADC for high speed CMOS image sensor was designed and implemented in a 0.18μm CMOS image sensor process. An opamp sharing technique is used to save area and power. Correlated double sampling circuit was integrated in the ADC core to remove the pixel FPN and two sets of capacitors were used in the cyclic ADC phase to accelerate the conversion speed. In order to reduce the column FPN, an offset cancellation technique was also adopted. The size of a single channel ADC is 20μm×1400μm and the power consumption from 1.8V supply is only 0.36mW. Measured results show the DNL and INL are +0.28 / -0.62 LSB and +2.1 / -2.1 LSB, respectively. Experimental results indicated that the ADC circuit is suitable for high-speed CMOS image sensor.

References